SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
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QUESTION BANK (DESCRIPTIVE)

Subject with Code: Switching Theory and Logic Design (20EC0403) **Course & Branch:** B.Tech & ECE

Year & Sem: II B.Tech & I Sem **Regulation:** R20

UNIT-I
BOOLEAN ALGEBRA AND LOGIC GATES

1.	a) Define Boolean Algebra and list the postulates used in it.	[L1][CO1]	[6M]
	b) State and prove any four Boolean theorems of Boolean algebra.	[L3][CO1]	[6M]
2.	State and prove the following Boolean laws: i) Commutative ii) Associative iii) Distributive	[L3][CO1]	[12M]
3.	a) Prove De Morgan's theorems using Perfect Induction Method.	[L3][CO1]	[6M]
	b) Simplify the given Boolean expression to a sum of 3 terms. A'C'D' +AC' +BCD + A'CD' + A'BC + AB'C'	[L4][CO2]	[6M]
4.	Simplify the following Boolean expressions: i) (X'+Z')(X+Y'+Z') ii) (X'Y' + Z)' + Z + XY + WZ iii) A'B(D' + C'D) + B(A +A'CD) iv) (A'+C)(A'+C')(A +B+C'D)	[L4][CO2]	[12M]
5.	a)Simplify the following Boolean functions to minimum number of literals: i)F_1 = (a + b)' (a' + b')' ii) F_2 = y(wz' + wz) + xy	[L4][CO2]	[6M]
	b) State and prove Consensus Theorem and Absorption Theorem of Boolean algebra.	[L3][CO1]	[6M]
6.	Identify the Dual of the following Boolean expressions. (i) AB'C+AB'D+A'B' (ii) A'B'C+ABC'+A'B'C'D	[L2][CO1]	[12M]
7.	Find the complement of the following Boolean expressions. i) B'C'D + (B + C + D)' + B 'C'D'E ii) AB + (AC)' + (AB + C) iii) A'B'C' + A'BC' + AB'C' + ABC' iv) AB + (AC)' + AB'C	[L3][CO1]	[12M]
8.	a) Express the following functions in Sum of Minterms and Product of Maxterms. i) F_1(A,B,C,D) = B'D + A'D + BD ii) F_2(x,y,z) = (xy + z)(xz+y)	[L2][CO1]	[6M]
	b) Express the following Boolean functions into Canonical form. i) F_1=AB+BC+CA ii)F_2= XY+Z+YZ+XYZ	[L2][CO1]	[6M]
9.	a) Simplify the given Boolean function, F to minimum number of literals using Boolean algebra. F=XY'Z + X'Y'Z +W'XY + WX'Y + WXY	[L4][CO1]	[6M]
	b) Draw the logic diagram for the simplified expression of the above using AOI logic.	[L1][CO2]	[6M]
10	a) List the different Boolean expressions for Two binary Variables.	[L1][CO1]	[6M]
	b) What are Universal Gates? Give their truth tables and Graphic symbols.	[L1][CO1]	[6M]

UNIT –II
GATE – LEVEL MINIMIZATION

1.	a) List the steps involved in simplification of K-Map.	[L1][CO1]	[6M]
	b) Simplify the Boolean expression, F=A'+AB+ABD'+AB'D'+C' using Four Variable K-Map and draw the logic diagram using AOI.	[L4][CO2]	[6M]
2.	a) Simplify the Boolean function using Five Variable K-Map. F=∑m(0, 1,2, 4, 7, 8, 12, 14, 15, 16, 17, 18, 20, 24, 28, 30, 31)	[L4][CO2]	[6M]
	Apply the K-Map technique to simplify the given Boolean expression in POS form using K-Map F(A,B,C,D) = Σ(1,2,4,5,9,12,13,14)	[L4][CO2]	[6M]
3.	a) Analyze the following Boolean function for minimal POS form using K-Map F(X,Y,Z) = X'YZ + XY'Z' + XYZ + XYZ'	[L4][CO4]	[6M]
4.	b) Deduce the given Boolean function using K-Map. F(A,B,C,D)=∑(1,3,7,11,15)+d(0,2,5)	[L4][CO2]	[6M]
	a) Simplify using K-Map and express the reduced expression in SOP and POS form. F = Σ m (0, 6, 8, 13, 14) + Σ d (2, 4, 10)	[L4][CO2]	[6M]
5.	b) Develop the logic diagram for the following Boolean function using NAND and NOR gates. Y=(AB'+A'B)(C+D').	[L3][CO5]	[6M]
	a) Explain the disadvantage of K-Map method of reducing a Boolean function and how to overcome it.	[L2][CO1]	[6M]
6.	Simplify the following expression using K-Map and realize with NAND and NOR gates. F = πM (1, 2, 3, 8, 9, 10, 11, 14). πd (7,15)	[L4][CO2]	[12M]
7.	a) Explain the structure of Ex-OR gate by K-Map using 4 Variable.	[L2][CO1]	[6M]
	b) Explain the Quine-Mc Cluskey method of minimizing the Boolean functions. Also mention its limitation.	[L2][CO1]	[6M]
8.	Simplify the following Boolean function by using Tabulation method. F = Σ (0, 1,2,8,10,11,14, 15)	[L4][CO2]	[12M]
9.	Determine the prime-implicants, essential prime implicants and simplified expression for the following function. F (w,x,y,z)= Σ (1,3,4,5,9,10,11) + Σd(6,8)	[L4][CO2]	[12M]
10.	Simplify the following Boolean function using Tabulation method, and realize its logic circuit with NAND gates and NOR gates. Y(A, B,C,D) = Σ(1,3,5,8,9,11,15)	[L4][CO2]	[12M]

UNIT –III
COMBINATIONAL LOGIC

1	a) Define Combinational Circuit and Explain the analysis procedure of a combinational logic circuit using suitable example.	[L2][CO1]	[6M]
	b) Explain the procedure of designing a combinational logic circuit with an example.	[L2][CO1]	[6M]
2	a) Define a Full Adder and realize it with use of truth table.	[L3][CO5]	[6M]
	b) Design a Full Subtractor using truth table.	[L3][CO5]	[6M]
3	a) Design a 4 bit parallel adder/ Subtractor using full adders.	[L3][CO5]	[6M]
	b) Design & implement a 4-bit Binary-to-Gray code converter.	[L3][CO4]	[6M]
4	a) Design a 4 bit Binary-to-BCD code converter.	[L3][CO4]	[6M]
	b) Construct a BCD Adder-circuit using 4-bit binary adders.	[L3][CO5]	[6M]
5	Explain Binary Multiplier with an example.	[L2][CO3]	[12M]
6	a) Explain a 2-bit Magnitude comparator and write down its design procedure.	[L2][CO3]	[6M]
	b) Design & implement Full Adder using Decoder.	[L3][CO4]	[6M]
7	a) Define Decoder and explain in detail about a 2 to 4 line binary decoder.	[L2][CO5]	[6M]
	b) Draw the circuit for 3 to 8 decoder and explain.	[L2][CO5]	[6M]
8	a) Illustrate the following Boolean functions using decoder and OR gates. $F1(A,B,C,D)=\sum(2,4,7,9)$ $F2(A,B,C,D)=\sum(10,13,14,15)$	[L3][CO5]	[6M]
	b) What is an encoder? Design an octal to binary encoder.	[L3][CO6]	[6M]
9	a) Define Multiplexer. Construct 4:1 multiplexer with logic gates and truth table.	[L3][CO4]	[6M]
	b) Represent the following Boolean function with an 8:1 multiplexer. $F(A,B,C,D) = A'BD'+ACD+B'CD+A'C'D$.	[L2][CO4]	[6M]
10	a) What is Demultiplexer? Design an1:8 demultiplexer using two 1:4 demultiplexer.	[L3][CO4]	[6M]
	b) Design a 32:1 Mux using two 16:1 MUXs and one 2:1 MUX.	[L3][CO4]	[6M]

UNIT –IV
SYNCHRONOUS SEQUENTIAL LOGIC

1.	a) Define a sequential logic circuit and sketch its block diagram.	[L1][CO1]	[4M]
	b) Differentiate between combinational and sequential circuits.	[L2][CO1]	[4M]
	c) Differentiate between synchronous and asynchronous sequential circuits.	[L2][CO1]	[4M]
2.	a) Define Latch and list different types of Latches.	[L1][CO1]	[4M]
	b) Define Flip-Flop. What are the different types of Flip-Flops?	[L1][CO1]	[4M]
	c) Explain the working principle of RS Flip-Flop with the help of logic diagram and give its Characteristic Table and Graphic symbol.	[L2][CO3]	[4M]
3.	a) With the help of logic diagram, obtain the characteristic table of D & T Flip-Flops. Also draw their graphic symbols.	[L2][CO3]	[6M]
	b) Explain the working principle of JK Flip-Flop in detail. Also give its characteristic equation, Graphic symbol and Excitation equation.	[L2][CO3]	[6M]
4.	a) Derive the characteristic equations for D & T Flip-Flops.	[L3][CO2]	[6M]
	b) Convert SR flip flop into JK Flip-Flop. Draw and explain its logic diagram.	[L2][CO4]	[6M]
5.	a) Design T Flip Flop using JK Flip-Flop and explain its logic diagram.	[L3][CO5]	[6M]
	b) Explain the steps involved in analysis of the clocked sequential circuits.	[L2][CO3]	[6M]
6.	a) Derive the excitation tables for SR, D, JK, and T Flip-Flops.	[L3][CO3]	[6M]
	b) Define a Shift register and explain its types.	[L2][CO1]	[6M]
7.	Design a 4 bit Decade counter.	[L4][CO6]	[12M]
8.	a) Define a counter and design a 4-bit Ripple counter.	[L1][CO6]	[8M]
	b) Explain in brief about a 2-bit synchronous up-counter.	[L2][CO6]	[4M]
9.	What is a synchronous counter? Design a 3-bit synchronous up/down counter.	[L4][CO6]	[12M]
10.	Explain about the following counters in detail. i) Ring counter ii) Johnson counter	[L2][CO3]	[12M]

UNIT –V
FINITE STATE MACHINES AND PROGRAMMABLE MEMORIES

<table>
<tr><td rowspan="3">1.</td><td>a) Define Mealy model and explain it with neat diagram.</td><td>[L1][CO1]</td><td>[4M]</td></tr>
<tr><td>b) Define Moore model. Explain it with neat diagram.</td><td>[L1][CO1]</td><td>[4M]</td></tr>
<tr><td>c) Distinguish between Mealy & Moore machines.</td><td>[L2][CO1]</td><td>[4M]</td></tr>
<tr><td>2.</td><td>Explain the following related to sequential circuits with suitable examples:
a) State diagram b) State table c) State assignment</td><td>[L2][CO1]</td><td>[12M]</td></tr>
<tr><td>3.</td><td>Derive the simplified sequential circuit for the following state table.
<table>
<tr><th rowspan="2">PS</th><th colspan="2">Next State</th><th colspan="2">Output</th></tr>
<tr><th>X=0</th><th>X=1</th><th>X=0</th><th>X=1</th></tr>
<tr><td>A</td><td>a</td><td>b</td><td>0</td><td>0</td></tr>
<tr><td>B</td><td>c</td><td>d</td><td>0</td><td>0</td></tr>
<tr><td>C</td><td>a</td><td>d</td><td>0</td><td>0</td></tr>
<tr><td>D</td><td>e</td><td>f</td><td>0</td><td>1</td></tr>
<tr><td>E</td><td>a</td><td>f</td><td>0</td><td>1</td></tr>
<tr><td>F</td><td>g</td><td>f</td><td>0</td><td>1</td></tr>
<tr><td>G</td><td>a</td><td>f</td><td>0</td><td>1</td></tr>
</table></td><td>[L3][CO6]</td><td>[12M]</td></tr>
<tr><td>4.</td><td>Determine the minimal state equivalent of the state table given.
<table>
<tr><th rowspan="2">PS</th><th colspan="2">Next State</th><th colspan="2">Output</th></tr>
<tr><th>X=0</th><th>X=1</th><th>X=0</th><th>X=1</th></tr>
<tr><td>A</td><td>a</td><td>b</td><td>0</td><td>0</td></tr>
<tr><td>B</td><td>c</td><td>g</td><td>0</td><td>1</td></tr>
<tr><td>C</td><td>a</td><td>d</td><td>0</td><td>0</td></tr>
<tr><td>D</td><td>e</td><td>f</td><td>0</td><td>1</td></tr>
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<tr><td>F</td><td>a</td><td>b</td><td>0</td><td>0</td></tr>
<tr><td>G</td><td>E</td><td>f</td><td>0</td><td>1</td></tr>
</table></td><td>[L3][CO6]</td><td>[12M]</td></tr>
<tr><td>5.</td><td>Explain in brief about Programmable Read Only Memory (PROM) with a suitable example.</td><td>[L2][CO2]</td><td>[12M]</td></tr>
<tr><td rowspan="2">6.</td><td>a) Compare ROM and RAM.</td><td>[L2][CO1]</td><td>[6M]</td></tr>
<tr><td>b) Classify various types of RAMs.</td><td>[L2][CO1]</td><td>[6M]</td></tr>
<tr><td>7.</td><td>Illustrate the PLA for the following Boolean function.
(i) $F_1 = \Sigma m(0,1,3,4)$ (ii) $F_2 = \Sigma m(0,1,2,3,4,5)$.</td><td>[L3][CO5]</td><td>[12M]</td></tr>
<tr><td>8.</td><td>Illustrate PLA for the following Boolean function.
$F_1(A,B,C) = \Sigma m(3,5,7)$
$F_2(A,B,C) = \Sigma m(4,5,7)$</td><td>[L3][CO5]</td><td>[12M]</td></tr>
<tr><td>9.</td><td>Illustrate the PAL for the following Boolean functions.
(i) $F(A,B,C,D) = \Sigma m(2,3,8,9,,10,12,13)$
(ii) $G(A,B,C,D) = \Sigma m(1,3,4,6,9,12,14)$</td><td>[L3][CO5]</td><td>[12M]</td></tr>
<tr><td>10.</td><td>Illustrate the PAL for the following Boolean functions.
(i) $A(w,x,y,z) = \Sigma m(0,2,6,7,8,9,12,13)$
(ii) $B(w,x,y,z)) = \Sigma m(0,2,6,7,8,9,12,13,14)$</td><td>[L3][CO5]</td><td>[12M]</td></tr>
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